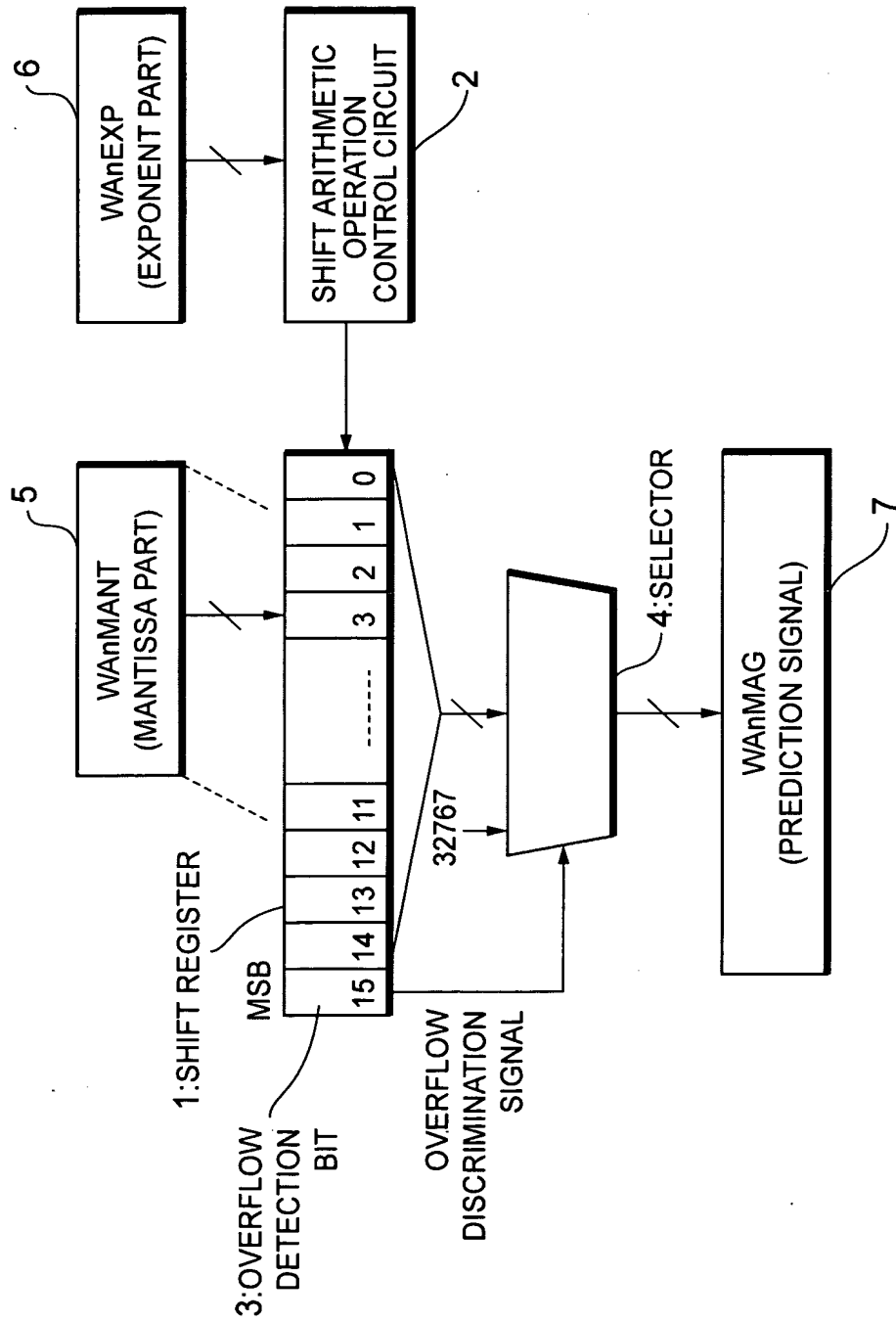


1/11

Fig.1



2/11

Fig. 2

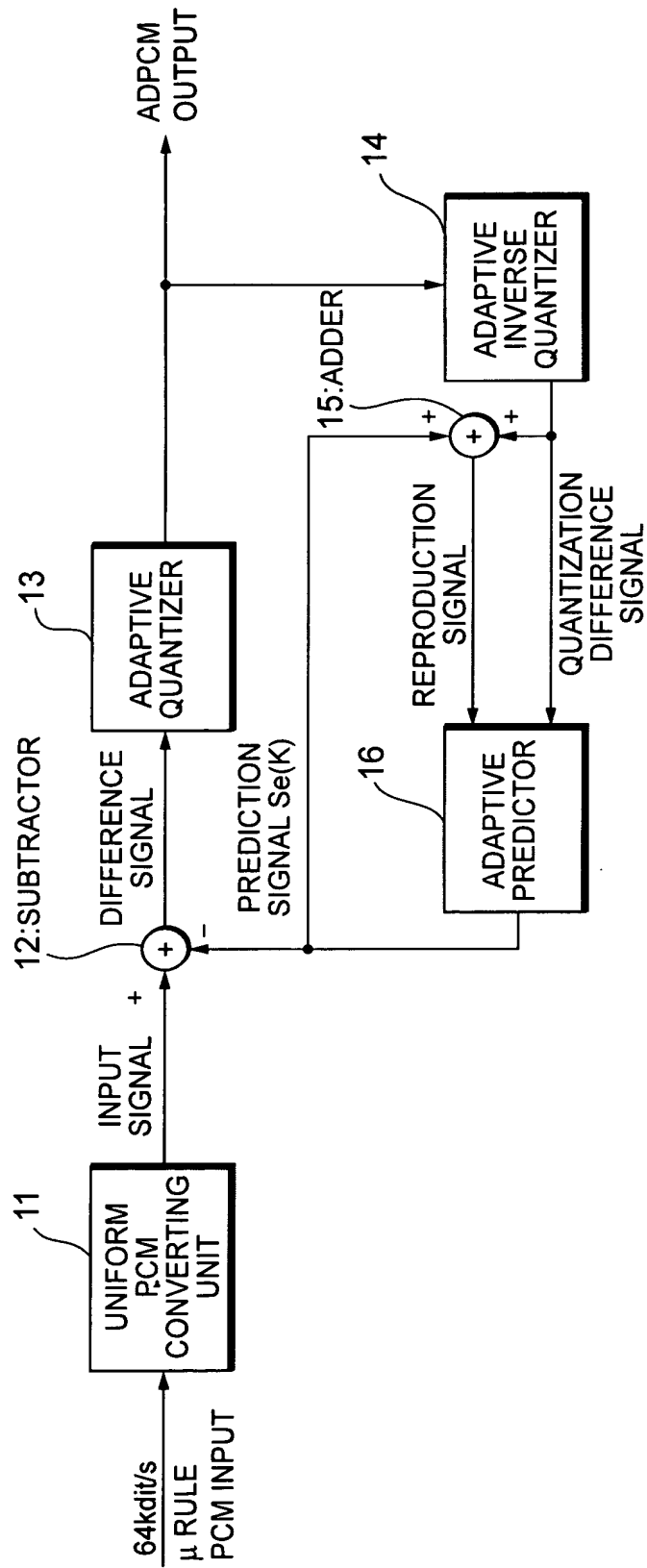
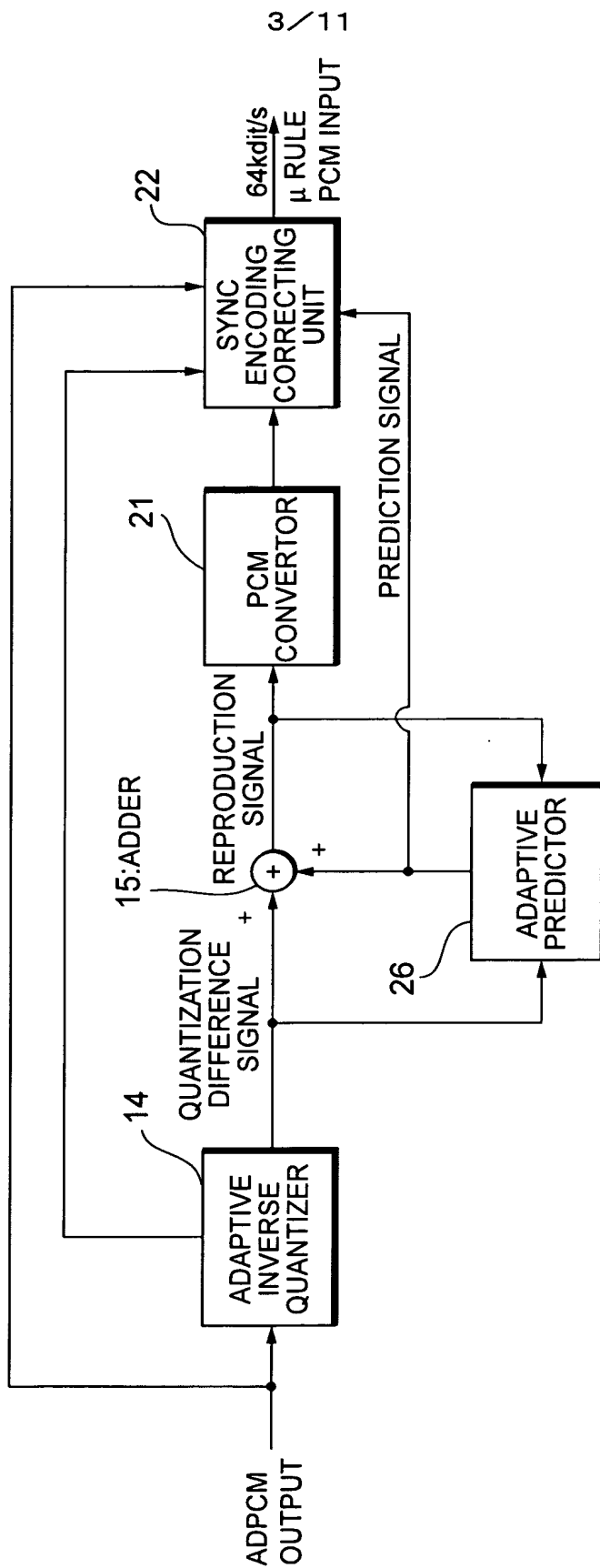


Fig.3



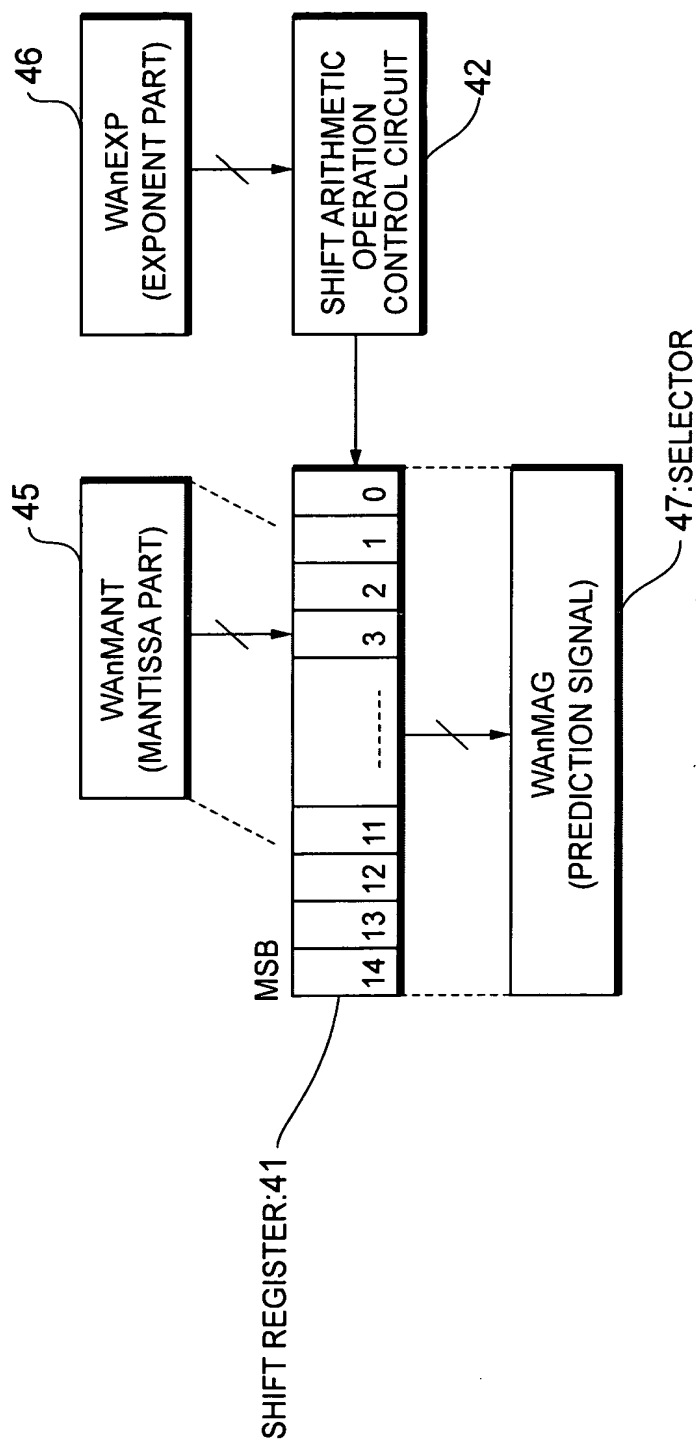
The diagram illustrates a complex digital signal processor (DSP) architecture. It features a central horizontal bar representing the main processing unit, with various functional blocks and registers connected to it. The architecture includes several stages of processing, such as addition, multiplication, and delay, as well as control logic and data paths. Key components include:

- Input/Output and Control:** Signals like SE, SIGPK, PK0, PK1, PK2, TR, WA1, WA2, and DQ are shown entering or leaving the system.
- Processing Blocks:** Functional blocks such as ADDC, DELAY, FMULT, TRIGB, LIMC, UPB, XOR, and UPB2 are distributed across the architecture.
- Registers and Buffers:** Numerous registers (R, SR0, SR1, SR2, DQ0-DQ6, WB1, WB6, A1, A2, A1R, A2R, A1P, A2P, A1T, A2T) and buffers (WB1, WB6) are used to store data and control signals.
- Accumulator:** A central ACCUM (Accumulator) block is shown, which likely accumulates the results of the processing stages.

The diagram is a detailed block-level representation of the DSP's internal structure, showing the flow of data and control signals through various processing stages.

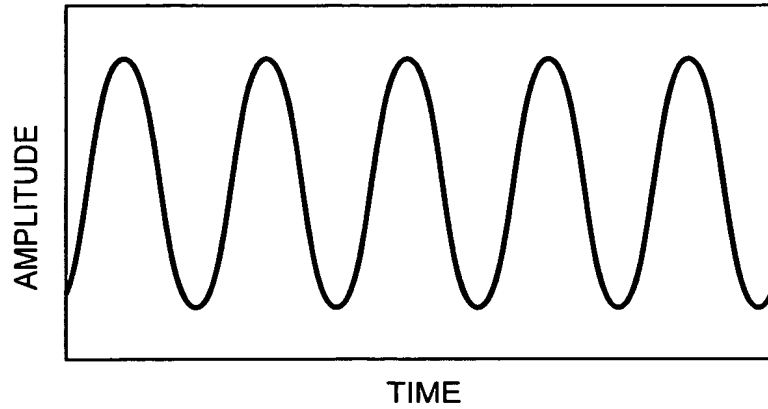
5/11

Fig. 5



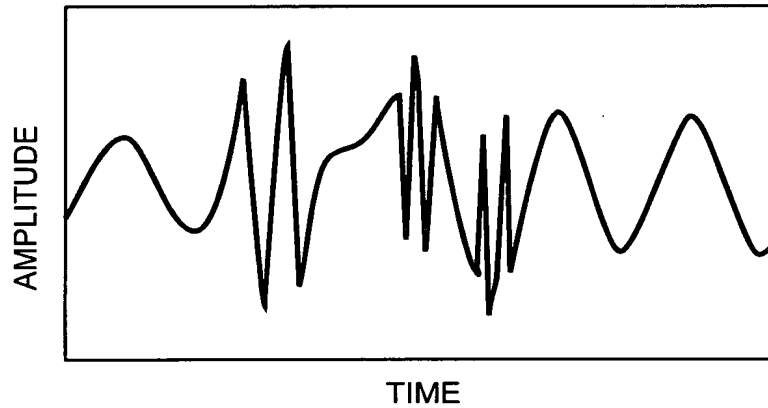
6/11

Fig. 6(a)



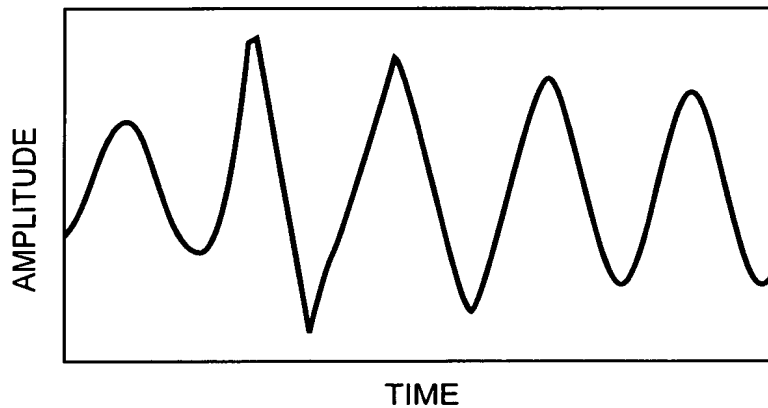
DECODER OUTPUT WHEN NORMAL DATA HAS BEEN DECODED

Fig. 6(b)



DECODER OUTPUT WHEN DATA HAVING ERRORS HAS BEEN DECODED

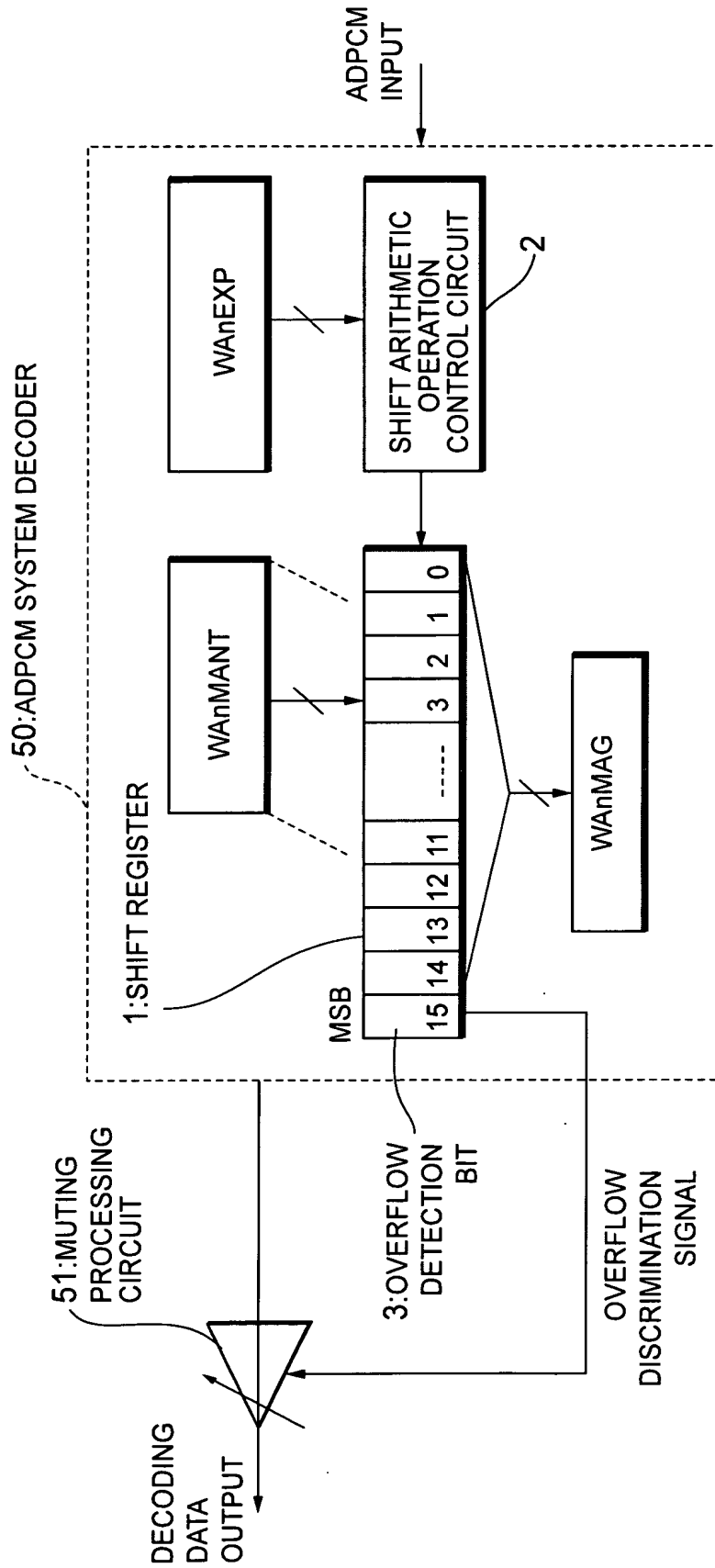
Fig. 6(c)



DECODER OUTPUT IN THE EMBODIMENT 1

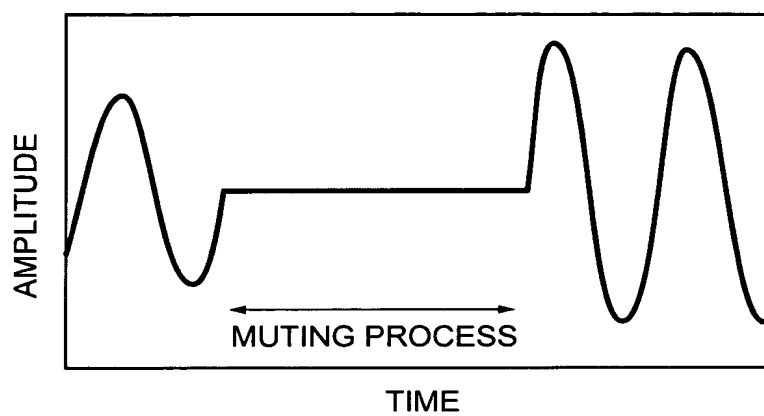
7/11

Fig.7



8/11

Fig. 8



9/11

Fig.9

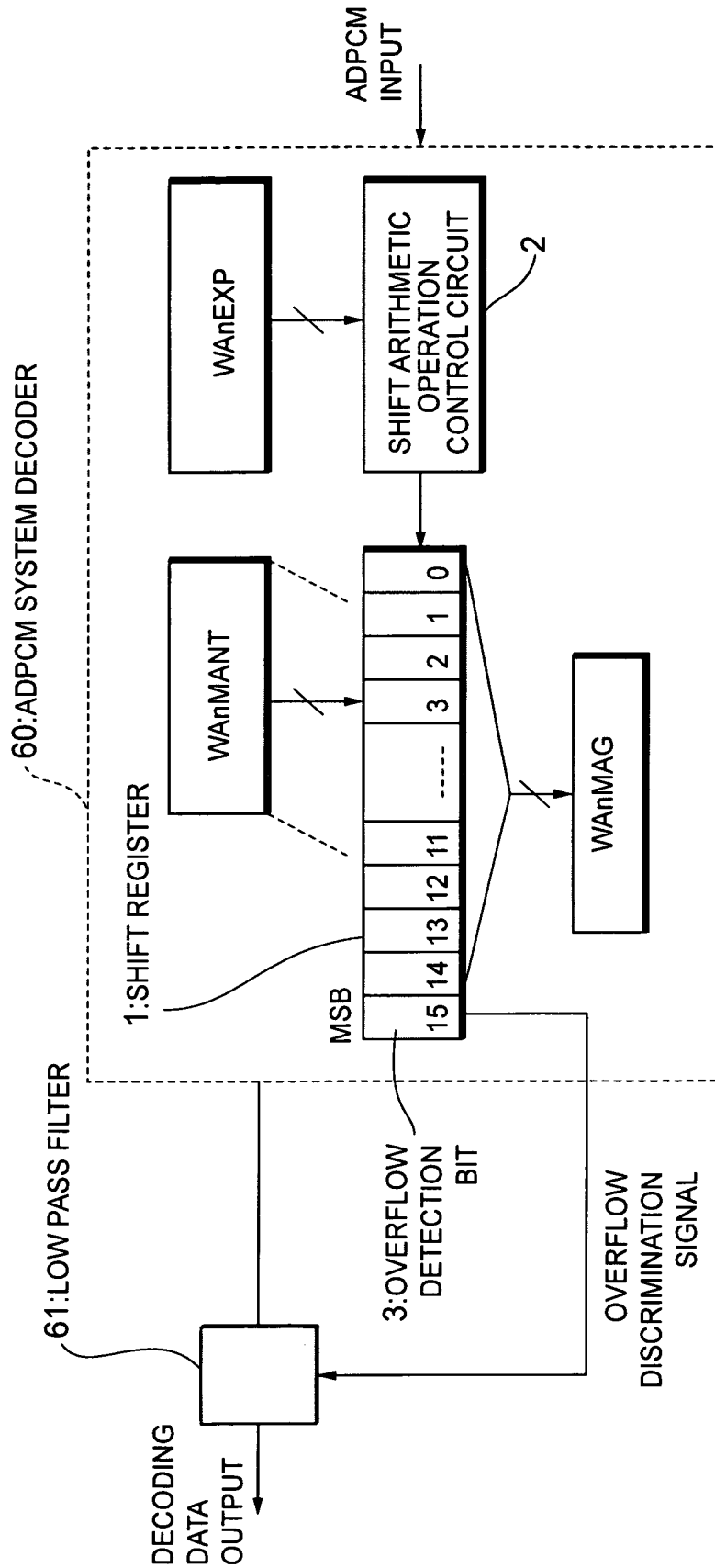


Fig.10

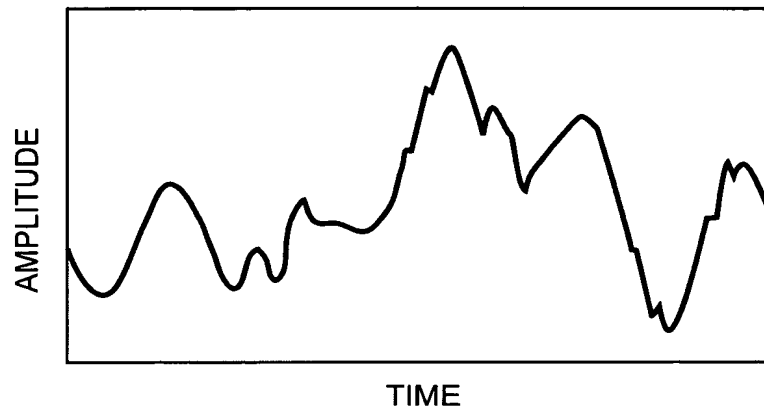


Fig. 11

NORMALIZED INPUT RANGE OF QUANTIZER $\log_2 D(k) -Y(k)$	$ D(k) $	NORMALIZED OUTPUT OF QUANTIZER $\log_2 D(k) -Y(k)$
[4.31, + ∞)	15	4.42
[4.12, 4.31)	14	4.21
[3.91, 4.12)	13	4.02
[3.70, 3.91)	12	3.81
[3.47, 3.70)	11	3.59
[3.22, 3.47)	10	3.35
[2.85, 3.22)	9	3.09
[2.64, 2.95)	8	2.80
[2.32, 2.64)	7	2.48
[1.95, 2.32)	6	2.14
[1.54, 1.95)	5	1.75
[1.08, 1.54)	4	1.32
[0.52, 1.08)	3	0.81
[-0.13, 0.52)	2	0.22
[-0.96, -0.13)	1	-0.52
[- ∞ , -0.96)	0	- ∞

INPUT/OUTPUT CHARACTERISTICS OF
THE ADAPTIVE QUANTIZER